INSA INSTITUT NATIONAL DES SCIENCES APPLIQUÉES LYON

DPT INFORMATIQUE
COMPUTER SCIENCE AND INFORMATION TECHNOLOGY
INSA Campus LyonTech - 7 Avenue Jean Capelle
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Hardware Architecture

Computer Architecture

IDENTIFICATION

CODE : IF-3-S1-EC-AO
ECTS : 2.0

HOURS

Lectures :	9.0 h
Seminars :	4.0 h
Laboratory :	12.0 h
Project :	0.0 h
Teacher-student contact :	25.0 h
Personal work :	25.0 h
Total :	50.0 h

ASSESSMENT METHOD

Written exam (1h30). Progress evaluation by Moodle QCM.

TEACHING AIDS

Lecture notes for the course, work sheets for classwork and labs (in French)

TEACHING LANGUAGE

French

CONTACT

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AIMS

The objective of this course is to understand
- the design and working principles of a modern computer (processor, memory hierarchy, peripherals)
- the lower levels of the software stack (assembly language, application binary interface, interruptions, input/output drivers, compiler).

Expected skills
- understanding the execution of a program or operating system on a machine
- low-level programming of embedded systems
- optimizing the execution of software for a given architecture (exploiting caches, instruction-level parallelism, etc)
- exploiting technical documentation in these fields

CONTENT

Lectures:
- design of a simple processor, from instruction set to architecture
- commented overview of current mainstream processors (x86, ARM, MSP430)
- exploiting instruction-level parallelism (pipeline, superscalar, SIMD)
- memory hierarchy and virtual memory

Classworks and labs
- building and simulating a processor
- MSP430 programming
- system aspects (I/O, interruptions)
- optimizing for performance (exploiting pipelines and caches)

BIBLIOGRAPHY

Tanenbaum. Computer architecture.

Hennessy & Patterson. Computer architecture, a quantitative approach.

PRE-REQUISITE

A basic course on digital circuits, for instance IF-3-AC